REMARKS

Claims 1-31 are pending. Independent claims 1, 19, and 27 were rejected under 35 U.S.C. 102(b) as being anticipated by Owen (USPN 4,876,660). Claims 1, 19, and 27 have been amended.

The Examiner argues that that the adder 34 in Owen is an arithmetic logic unit and the accumulators 40 and 42 in Owen are a plurality of registers. The Examiner also argues that in the alternative, Adder 34 in combination with MUX 62 is an arithmetic logic unit. The Applicants respectfully disagree. As noted in the previous Office Action Response, an arithmetic logic unit is a significant component of a processor and is operable to perform addition, subtraction, bit shifting operations, and logic operations, not merely addition. Nonetheless, the independent claims 1, 19, and 34 have been amended to clarify that the arithmetic logic unit is "operable to perform arithmetic and bit shifting operations."

Furthermore, the independent claims 1, 19, and 34 have been amended to recite "the arithmetic logic unit is operable to read data and carry flag information from one of the plurality of registers and write data and carry flag information to one of the plurality of registers." The Adder 34 does not perform this recitation. Similarly, the Adder 34 in combination with MUX 62 does not perform this recitation.

In light of the above remarks, the rejections to the independent claims are believed overcome for at least the reasons noted above. Applicants believe that all pending claims are allowable in their present form. Please feel free to contact the undersigned at the number provided below if there are any questions, concerns, or remaining issues.

Respectfully submitted,
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